

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of)	
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Dave STUTTARD, <i>et al.</i>)	Group Art Unit: Unassigned
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Application No.: Unassigned)	Examiner: Unassigned
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Filed: 09 October 2001)	
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For: PARALLEL DATA PROCESSING)	
APPARATUS)	

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Prior to examination, please amend the above-identified application as follows:

IN THE SPECIFICATION:

After the Title, please add the following paragraph:

This application is a continuation of PCT International Application No.

PCT/GB00/01332, filed on 07 April 2000 and published by the International Bureau in the English language as International Publication No. WO 00/62182 on 19 October 2000. PCT International Application No. PCT/GB00/01332 claims priority from the following applications filed in Great Britain on 09 April 1999: 9908199.4; 9908201.8; 9908203.4; 9908204.2; 9908205.9; 9908209.1; 9908211.7; 9908214.1; 9908219.0; 9908222.4; 9908225.7; 9908226.5; 9908227.3; 9908228.1; 9908229.9; and 9908230.7, which are hereby incorporated by reference into the present document. International Publication No. WO 00/62182 is hereby incorporated by reference into the present document.

IN THE CLAIMS:

Please cancel claim 89.

Please replace amended claims 3, 5, 7-8, 12-15, 18, 20-21, 23, 26-28, 30-32, 34-36, 38-40, 42, 44, 46-47, 50, 52-56, 59-60, 62, 64, 69, 71-73, 75, 78-80, 82-86, 99, 101-102, 110, 115-116, 124, 126, 132, 135, 138-139, 142-144, 147-149, 151, 155, 157-158, 160-161, 164-166, 168-169, 173-179, 184, 188, 192, 194, 196-197, 201-202 and 205 as follow:

3. An apparatus as claimed in claim 1, wherein at least one of the processing blocks is a redundant block operable to process a group of data items in place of a faulty processing block.

5. An apparatus as claimed in claim 1, wherein each processing block is provided with at least one redundant processing element operable to process data items in place of a faulty processing element of the block concerned.

7. An apparatus as claimed in claim 5, comprising fault detection means operable to detect a fault occurring in a processing element and to transfer the data processing function of that processing element to a redundant processing element.

8. An apparatus as claimed in claim 1, wherein each processing block includes a mathematical expression evaluator which is operable to evaluate a mathematical

expression for each processing element and to provide respective evaluations to the processing elements in the processing block.

12. An apparatus as claimed in claim 1, wherein instructions and data items to be processed by the processing elements are supplied separately from one another to the processing elements.

13. An apparatus as claimed in claim 1, wherein the data items to be processed by processing elements in a processing block are supplied by processing elements in that processing block.

14. An apparatus as claimed in claim 1, wherein each processing element comprises a processing unit for receiving data items and instruction items, which processing unit is operable to process the data items according to received instruction items, a memory unit for storing data items received from the processing unit, and a register file arranged between the processor unit and the memory unit, which register file is operable to store data items from the processor unit and from the memory unit, for transfer to the other of those units and is operable to store data items for processing by the processor unit of the processing element.

15. A data processing apparatus as claimed in claim 1, comprising an external memory for storing data items and instruction items; and

a controller means for controlling transfer of data and instruction items between each processing element and the external memory,

wherein the or each processing element comprises:

a processor unit connected to receive data items and instruction items and operable to process the said data items in accordance with the said instruction items;

a plurality of storage registers for temporarily storing data items for input to the processor unit, at least one of the storage registers being operable to store an offset value;

a memory unit for storing data items and address data indicating an external memory address; and

a register file for storing data items, the register file being connected between the processor unit and the memory unit for receiving data items from either of those units for transfer to the other of those units, and for transferring data items with memory external to the processing element, and for storing data items for processing by the processor unit, and

wherein the controller is operable to retrieve an offset value from the storage registers, to combine the offset value with a predetermined reference address to give a calculated internal address, to retrieve external address data stored at the calculated internal address in the internal memory, and to access the external memory at the external address.

18. A data processing apparatus as claimed in claim 1, wherein each processing element comprises:

a processor unit for processing data items in accordance with instruction items; and
an enable register for indicating whether the element is available for processing data items,

the enable register including a plurality of indicators, each operable to indicate an enabled or disabled condition of the processing element, the processing element being available for processing of data items when all said indicator units indicate the enabled condition.

20. A data processing apparatus as claimed in claim 18, wherein the enable register is provided by a hardware register.

21. A data processing apparatus as claimed in claim 1, wherein each processing element in the array is operable to transfer data items directly with at least one neighbouring processing element, and wherein each processing block includes a processing element which is operable to transfer data items directly with a processing element in another processing block.

23. A data processing apparatus as claimed in claim 21, wherein the processing elements are provided on a single integrated circuit.

26. A data processing apparatus as claimed in claim 24, wherein the processing blocks are connected in a series, the last processing element of a processing block, being operable to transfer data with the first processing element in another processing block in the series.

27. A data processing apparatus as claimed in claim 24, wherein the processing blocks are connected in a series, the last processing element of a processing block, except the last processing block in the series, being operable to transfer data with the first processing element in the next processing block in the series.

28. A data processing apparatus as claimed in claim 1, comprising a controller which includes:

means for retrieving instruction items for each of a plurality of instruction streams;

means for combining the plurality of instruction streams into a serial instruction stream; and,

means for distributing the serial instruction stream to either a processing controller which controls data processing of the array of processing elements, or a data transfer controller which controls the transfer of data to and from the processing elements.

30. A data processing apparatus as claimed in claim 28, comprising:
a plurality of instruction stream processors, one for each instruction stream, for controlling the respective instruction streams;

a semaphore controller for controlling synchronisation between instruction streams;
a status block for providing status information regarding each of the instruction streams;
and
a scheduling means connected to receive status information, and operable to
determine which of the instruction streams is to be active.

31. A data processing apparatus as claimed in claim 28, wherein each instruction stream is assigned a relative priority level.

32. A data processing apparatus as claimed in claim 1, comprising a semaphore controller which includes:
means for maintaining synchronism between the execution of the plurality of separate instruction streams.

34. A data processing apparatus as claimed in claim 32, having means for decrementing a semaphore value.

35. A data processing apparatus as claimed in claim 32, having means for incrementing a semaphore value.

36. A data processing apparatus as claimed in claim 32, having means for arranging the semaphores into a plurality of groups.

38. A data processing apparatus as claimed in claim 32, having means for controlling the access of a plurality of instruction streams to a shared resource.

39. A data processing apparatus as claimed in claim 32, having means for incrementing and/or decrementing semaphore values in response to instructions issued by a processor.

40. A data processing apparatus as claimed claim 1, comprising an array controller which includes means connected to receive instructions, and routing means operable to transfer received instructions to the array of processing elements in dependence upon the instruction concerned.

42. A data processing apparatus as claimed in claim 40, wherein the routing means comprises:

a processing element instruction sequencer for handling data processing instructions which relate to processing of data by the processing elements; and

a data transfer controller for handling data transfer instructions which relate to the transfer of data items to and/or from the processing elements.

44. A data processing apparatus as claimed in claim 40, wherein each processing element further comprises a set of registers, and wherein the instruction launcher includes means for determining which registers of the processing elements are accessed by an

instruction, and means for preventing other instructions from accessing these registers while the instruction is being performed.

46. A data processing apparatus as claimed in claim 40, further comprising an instruction table for assisting the instruction launcher in determining which registers are accessed by data processing instructions.

47. A data processing apparatus as claimed in claim 40, wherein the instruction launcher maintains the appearance of serial execution, while also maintaining parallel operation between the processing element instruction sequencer and the data transfer controller.

50. A data processing apparatus as claimed in claim 40, wherein the data transfer controller comprises control means operable to control transfer of data to and/or from an internal memory unit of a processing element in a SIMD (single instruction multiple data) array of processing elements, each processing element including a processing unit and an internal memory unit, the control means being operable such that data transfer to and/or from the internal memory unit is performed independently of the operation of the processing unit of the processing element concerned.

52. A data processing apparatus as claimed in claim 50, further comprising a mathematical expression evaluator (MEE), and wherein the data transfer controller has

means for controlling transfer of data between the internal memory unit of a processing element and the expression evaluator.

53. A data processing apparatus as claimed in claim 50, wherein the data transfer controller has means for transferring data between the internal memory unit of one processing element and the internal memory unit of another processing element.

54. A data processing apparatus as claimed in claim 50, wherein the data transfer controller has means for performing a memory refresh on the internal memory units of the processing elements.

55. A data processing apparatus as claimed in claim 50, wherein the data transfer controller has means for performing transfer of data between an internal memory unit of a processing element and memory external to the processing element.

56. A data processing apparatus as claimed in claim 1, comprising:
a local memory unit for storing data items for transfer to and from the processing elements, the data items' being stored at addresses in the memory unit; and
a segment register for each processing block, for storing segment information relating to the local memory unit, the segment information indicating the address area of the local memory unit to be accessed by the processing block concerned.

59. A method of processing data using data processing apparatus as claimed in claim 1 and a local memory unit for storing data items at addresses in the local memory unit, the method comprising:

supplying an instruction item to the processing elements, the instruction item including address information relating to data items stored in the local memory unit;

obtaining segment information for each processing block, the segment information relating to the address area of the local memory unit to which a processing block has access;

combining the segment and address information to produce target address information; and

accessing the local memory unit on the basis of the target address information.

60. A data processing apparatus as claimed in claim 1, wherein each processing element comprises a processor unit, a memory input/output port for transferring data items to and from a data storage unit, and a set of data registers for transferring data items to the processor unit, wherein each of the registers in the set of data registers is connected for receiving data items from the memory input/output port, and for receiving data items from an output of the processor unit, and for transferring data items to an input of the processor unit.

62. A data processing apparatus as claimed in claim 60, comprising a data shifter connected to receive input data items from three of the said data registers, and operable to shift received data items by a predetermined number of data bits, and to transfer shifted data items to the three data registers.

64. A data processing apparatus as claimed in claim 60, wherein the processing unit comprises an arithmetic logic unit.

69. A method as claimed in claim 68, comprising the steps of:
determining whether an instruction stream with higher priority than the currently active stream is ready to execute; and,
if a higher priority instruction stream is ready to execute, activating the instruction stream having the higher priority.

71. A method of controlling data read access to memory in a data processing apparatus as claimed in claim 1, the method comprising:
selecting a processing element that requires access to the memory,
retrieving a target address from the selected processing element,
transmitting the target address to the plurality of processing elements,
transmitting transaction identification information to the processing elements, which information identifies the target address access operation concerned,

storing the transaction identification information in the or each processing element that requires access to the target address,

transmitting data obtained from the target address together with the transaction identification information to the plurality of processing elements, and

storing the obtained data in the or each processing element in which the transaction identification information is stored.

72. A method of retrieving a data item from a memory unit in a data processing apparatus as claimed in claim 1, and which includes a memory unit in which data items are stored at addresses therein, and a plurality of processing elements which have access to the memory unit, the method comprising:

for each processing element in the array which requires access to the memory unit, setting an access indicator to indicate that the processing element concerned requires access to the memory unit, and storing a target address of the memory unit to which such access is required;

selecting one of the processing elements having the access indicator set, and retrieving the stored target address from that selected processing element;

transmitting the retrieved target address and transaction identification information to the processing elements in the array;

for each processing element having the access indicator set, comparing the transmitted target address with the stored target address, and if the stored and transmitted